MOS Transistor Matching

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Device Size Optimized for Current Match or Voltage Match?

- Differential pair – require $V_{GS}$ matching
- Current mirror – require $I_D$ matching

✓ Subthreshold  

$$I_D = I_0 \exp \left( \frac{V_{GS}}{\xi kT/q} \right)$$

✓ Strong inversion  

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

✓ Current input $\Rightarrow$ small $\Delta V_{GS}$  

✓ Voltage input $\Rightarrow$ small $\Delta I_D$
Geometric Effects

- Large transistors match better than small transistors
  - Fluctuations average out over larger area
- Long channel transistors match better than short
  - Less Channel length modulation effects
- Identically oriented transistors match better
  - Silicon is anisotropic and hence has different conductance in different directions

\[
\sigma_{Vt} = \frac{C_{Vt}}{\sqrt{W_{ef} L_{ef}}} \quad \quad \sigma_{Gm} = \frac{C_{Gm}}{\sqrt{W_{ef} L_{ef}}}
\]
Geometric Effects

- Transistors with thinner gate oxides match better (assuming same area)
  - Higher back gate doping fluctuations average out over larger area
  - Edge fringing effects are less pronounced

- Transistor orientation is important
Etch Effects

- Polysilicon does not always etch uniformly
  - Large openings etch faster than small openings in mask
  - Solution is to use dummy structures
Diffusion Effects

- Diffusion widens implanted region
  - Can affect doping of neighboring devices
  - Solution is to increase distance and use dummy structures that affect all transistors the same
Thermal Effects

- Temperature affects
  - Mobility and threshold voltage
  - Resistance value
**Stress Effects**

- The fabrication under high temperatures may leave residual stresses in chip
- Packaging can cause stress in chip

**Solutions**

- Keep critical matched devices in centre of chip or on centerlines
- Avoid using corners for matched devices
Oxide Thickness Gradients

- Thermally grown oxides depend on temperature and oxidizing atmosphere
- Modern oxidation furnaces, although well controlled in temperature still have temperature gradients.

Oxide thickness on 200 mm wafer
Dealing with Large transistors

- These can be split into many parallel fingers
- Contact space is shared amongst transistors
- Parasitic capacitance is reduced
Transistor Matching?

- Example of Differential Pair
  - ✗ Not matching with thermal gradients!!!

![Diagram of differential pair with process variations and mismatched transistors]
Common Centroid Layouts

- Matching Won’t be good!!!
Common Centroid Layouts

- Break and distribute parts of a transistor so as to cancel out the effects of oxide / doping gradient profiles.

M1 Average Thickness = 4.5nm  M2 Average thickness = 4.5nm
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Common Centroid Layouts

- Averages Process Variations
Common Centroid Layouts

- Averages Process Variations

![Diagram showing common centroid layouts with labels M1 and M2 arranged in a 4x4 grid. The centroid is marked by a black dot.](image)
Create Floorplan before Implementing Layout

- M1 and M2 must match
- M3 and M4 must match, M6 must be wider by 4xM3
- M7 must be 2x M5

Pay attention to your floor plan! It is critical for minimizing iterations: Identify the critical elements.
Example Common Centroid Layout

- Industrial Quality
  - Includes multiple guards
  - Full common centroid
  - Dummy structures
Other good practices

- Avoid placing contacts over active gate area
- Avoid routing metal over gate
- Use identical finger geometries
- Place transistors in close proximity
- Avoid using extremely short or narrow transistors
- Connect gate areas using metal straps