The Devices
July 30, 2002

Goal of this chapter

- Present intuitive understanding of device operation
- Introduction of basic device equations
- Introduction of models for manual analysis
- Introduction of models for SPICE simulation
- Analysis of secondary and deep-sub-micron effects
- Future trends
The Diode

Cross-section of p-n junction in an IC process

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Depletion Region

(a) Current flow.
(b) Charge density.
(c) Electric field.
(d) Electrostatic potential.

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Diode Current

\[ I_D = I_S \left(e^{V_D/\Phi_T} - 1\right) \]

Forward Bias

Typically avoided in Digital ICs
Reverse Bias

The Dominant Operation Mode

Models for Manual Analysis

(a) Ideal diode model

(b) First-order diode model
### Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - W_D / W_0)^m} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction

### Diffusion Capacitance

\[ C_d = \frac{dQ_D}{dV_D} = \frac{\tau_d V_D}{\tau_d V_D + \frac{V_D}{qT}} \]
Secondary Effects

Avalanche Breakdown

Diode Model
### SPICE Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation current</td>
<td>( I_c )</td>
<td>IS</td>
<td>A</td>
<td>1.0 E-14</td>
</tr>
<tr>
<td>Emission coefficient</td>
<td>( n )</td>
<td>N</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Series resistance</td>
<td>( R_S )</td>
<td>RS</td>
<td>( \Omega )</td>
<td>0</td>
</tr>
<tr>
<td>Transit time</td>
<td>( \tau_T )</td>
<td>TT</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Zero-bias junction capacitance</td>
<td>( C_JJ )</td>
<td>CJ0</td>
<td>F</td>
<td>0</td>
</tr>
<tr>
<td>Grading coefficient</td>
<td>( m )</td>
<td>M</td>
<td></td>
<td>0.5</td>
</tr>
<tr>
<td>Junction potential</td>
<td>( \phi_0 )</td>
<td>VJ</td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

First Order SPICE diode model parameters.

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### What is a Transistor?

A Switch! \( V_{GS} \geq V_T \) \[ \Rightarrow \] An MOS Transistor

\[ |V_{GS}| \]
The MOS Transistor

MOS Transistors - Types and Symbols

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Threshold Voltage: Concept

![Diagram of a transistor showing n-channel depletion region]

The Threshold Voltage

\[ V_T = \phi_{\text{mS}} - 2\phi_F \left( \frac{Q_B}{C_{OX}} \right) - \frac{Q_{GR}}{C_{OX}} - \frac{Q_I}{C_{OX}} \]

Workfunction Difference

Surface Charge

\[ V_T = V_{T0} + \gamma \left( \sqrt{\frac{-2\phi_F + V_{BE}}{2\phi_F}} - \sqrt{-2\phi_F} \right) \]

Body Effect Coefficient

\[ V_{T0} = \phi_{\text{mS}} - 2\phi_F \left( \frac{Q_{GS}}{C_{OX}} \right) - \frac{Q_{DS}}{C_{OX}} - \frac{Q_I}{C_{OX}} \]

and

\[ \gamma = \frac{\sqrt{qE_{ox}N_A}}{C_{OX}} \]
The Body Effect

Current-Voltage Relations
A good ol' transistor
**Transistor in Linear**

MOS transistor and its bias conditions

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**Transistor in Saturation**

Pinch-off

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Current-Voltage Relations
Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k_n \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}$$

with

$$k_n = \mu_n C_{ox} \frac{L}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} > V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k_n W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

A model for manual analysis

$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k_n W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$V_{DS} \leq V_{GS} - V_T$$

$$I_D = k_n \frac{W}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}$$

with

$$V_T = V_{T0} + \gamma \left( 2\Phi_p + V_{SB} - 2\Phi_C \right)$$
Current-Voltage Relations
The Deep-Submicron Era

Velocity Saturation

\[ \nu_n (\text{m/s}) \]

\[ \xi (\text{V/\mu m}) \]

\[ \xi_c = 1.5 \]

\[ \nu_{sat} = 10^5 \]

Constant velocity

Constant mobility (slope = \( \mu \))

\[ \xi_c = 1.5 \]

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Perspective

Long-channel device

Short-channel device

V_{GS} = V_{DD}

I_{D} versus V_{GS}

Long Channel

Short Channel

I_{D} (A) versus V_{GS} (V)

quadratic

linear
$I_D$ versus $V_{DS}$

A unified model for manual analysis

\[ I_D = 0 \text{ for } V_{GT} \leq 0 \]

\[ I_D = k'W \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) \left( 1 + \lambda V_{DS} \right) \text{ for } V_{GT} \geq 0 \]

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{2}\phi_F + V_{SB}) - \sqrt{2}\phi_F$
Simple Model versus SPICE

A PMOS Transistor

Assume all variables negative!
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device):

<table>
<thead>
<tr>
<th></th>
<th>$V_{th}$ (V)</th>
<th>$\gamma$ (V$^{0.5}$)</th>
<th>$V_{SSAT}$ (V)</th>
<th>$K$ (A/V$^2$)</th>
<th>$\lambda$ (V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-4}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

The Transistor as a Switch

$$R_{on} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSS}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSS}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSS}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)$$
The Transistor as a Switch

Table 3.3 Equivalent resistance $R_{on}$ (W/L = 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide $R_{on}$ by W/L.

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>
MOS Capacitances
Dynamic Behavior

Dynamic Behavior of MOS Transistor
The Gate Capacitance

Polysilicon gate

Cross section

Gate Capacitance

Operation Region | $C_{Gφ}$ | $C_{GS}$ | $C_{GD}$
--- | --- | --- | ---
Cutoff | $C_{ox}WL_{eff}$ | 0 | 0
Triode | 0 | $C_{ox}WL_{eff} / 2$ | $C_{ox}WL_{eff} / 2$
Saturation | 0 | $(2/3)C_{ox}WL_{eff}$ | 0

Most important regions in digital design: saturation and cut-off
Gate Capacitance

Capacitance as a function of VGS (with VDS = 0)

Capacitance as a function of the degree of saturation

Measuring the Gate Cap

Gate Capacitance (F)

Gate Capacitance (F)

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**Diffusion Capacitance**

Channel-stop implant

\[ C_{diff} = C_{bottom} + C_{sw} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER} \]
\[ = C_j L_s W + C_{jsw} (2L_s + W) \]

**Junction Capacitance**

\[ C_j = \frac{C_{j0}}{1 - \frac{V_D}{I_D} I_{D0}} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction
**Linearizing the Junction Capacitance**

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest.

\[ C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C \phi \]

\[ K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} [(\phi_0 - V_{high})^{1-n} - (\phi_0 - V_{low})^{1-n}] \]

**Capacitances in 0.25 μm CMOS process**

<table>
<thead>
<tr>
<th></th>
<th>( C_{ox} ) (( \text{fF/\text{\mu m}^2} ))</th>
<th>( C_0 ) (( \text{fF/\text{\mu m}^2} ))</th>
<th>( C_j ) (( \text{fF/\text{\mu m}^2} ))</th>
<th>( m_f )</th>
<th>( \phi_0 ) (( V ))</th>
<th>( C_{oxw} ) (( \text{fF/\text{\mu m}} ))</th>
<th>( m_{fsw} )</th>
<th>( \phi_{sw} ) (( V ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>
The Sub-Micron MOS Transistor

- Threshold Variations
- Subthreshold Conduction
- Parasitic Resistances

**Threshold Variations**

![Graph showing threshold variation as a function of length and drain-source voltage.](image)
**Sub-Threshold Conduction**

The Slope Factor

\[ I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}} \]

\[ S = n \left( \frac{kT}{q} \right) \ln(10) \]

Typical values for S: 60 .. 100 mV/decade

**Sub-Threshold**

\[ I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left( 1 - e^{-\frac{qV_{GS}}{nkT}} \right) \]

\[ V_{DS} \text{ from 0 to 0.5V} \]
**Sub-Threshold** $I_D$ vs $V_{DS}$

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{nkT}}\right)(1 + \lambda \cdot V_{DS})$$

**Summary of MOSFET Operating Regions**

- **Strong Inversion** $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$

- **Weak Inversion (Sub-Threshold)** $V_{GS} \leq V_T$
  - Exponential in $V_{GS}$ with linear $V_{DS}$ dependence
Parasitic Resistances

Latch-up
Future Perspectives

25 nm FINFET MOS transistor