MemoCIS 1st Workshop and MC Meeting
'Memristors – Devices, Models, Circuits, Systems and Applications', Lisbon, Portugal.
9.-11.5.2015

PROGRAM
Day 1 - Thursday, May 28, 2015

08:30 – 09:00 Registration and Welcome

09:00 – 10:00 Keynote: Daniele Ielmini “Resistive switching devices: switching, reliability and novel applications”

Resistive switching (RS) devices are attracting a great deal of interest for future generations of memory and computing due to scalable device size, high speed and low power consumption. One of the key obstacle toward developing a feasible RS technology is the immature understanding of switching mechanisms and scalability. This talk will review the recent progress on the physical modeling of RS operation based on ionic migration driven by electric field and local Joule heating. Device reliability and scaling limitations will be discussed in terms of Poissonian defect fluctuations causing noise, switching variability and cycling endurance. Finally, the potential applications in computing will be considered in terms of logic computing (beyond-CMOS logic, random number generation) and neuromorphic synapses capable of unsupervised pattern recognition.

10:00 – 10:30 Yakov Roisin "Single Poly Memristor-Like Devices in CMOS Process Flows"

The talk is devoted to single Poly EEPROMs that have performance similar to memristors. Single Poly memristor-like devices with relatively small footprints can fabricated in a standard CMOS process flow without additional masks. The resistance of these devices is much more stable than for ReRAM type memristors. Several types of single Poly NVMs with enhanced reliability developed in TowerJazz will be reported and their performance discussed. One of the possible applications is acting as artificial synapses in neuromorphic circuits with neurons imitated by CMOS elements.
10:30 – 11:00  
Coffee Break

11:00 – 11:20  
**Martin Klimo, Ondrej Such, Eike Linn**  “Fuzzy logic with memristors”

Linear models of memristors allow building models of elementary memristive circuits for functions of minimum, maximum and average in analog mode. Nonlinear models and real measurements show that behavior of memristors is (due to non-linearity of the switching kinetics) much more complex and working area for fuzzy logic calculation is more narrow. Presentation will show why some problems in multilayer memristive circuits can be expected. On the other side the working area that is not suitable for fuzzy logic can be used for switching and signal routing. In this way the memristive circuits can combine two functionalities: switching and processing within the same circuit.

11:20 – 11:40  
**Antony Kenyon**  “Silicon oxide – a dynamic Electronic Material for Resistance Switching”

Silicon oxide has for many years provided engineers with an ideal insulator. Silicon microelectronics still relies on its physical, chemical and, above all, electrical durability; modern devices incorporate few-nanometre thick oxide layers in which the electrical stress can be extreme. Here, we report the highly dynamic structural and electrical behaviour of thin silicon oxide films under voltage stress. We show, using a combination of electrical measurements, structural measurements, in situ ion detection and mass spectroscopy, along with DFT and Monte Carlo models, that realistic device voltages can generate major changes to the oxide that are reflected in high contrast resistance switching. In some cases these changes are reversible; in others they are permanent precursors to dielectric breakdown. Our results have major implications for the use of silicon oxide in electronics and photonics – rather than a passive, stable insulator prior to breakdown it is instead a highly dynamic electrically manipulated system.
Eleni Vasilaki "Synaptic dynamics and STDP in Neural Networks and Memristive devices"

I will discuss how interaction of short-term and long-term plasticity leads into non-random connectivity motifs, as observable in electrophysiology experiments. I will further discuss collaborative work with the University of Southampton (Prodromakis group) that lead to the design of memristive devices with properties akin to chemical synapses, that are able to qualitatively reproduce long term plasticity experiments and exhibit short-term plasticity properties. These key characteristics may lead to the formation of desirable connectivity motifs in memristive neural networks.

Adnan Mehonic, M. Buckwell, L. Montesi, M. Singh Munde, S. Hudziak, A. J.Kenyon
“Silicon Oxide as an Intrinsic Resistance Switching Material”

We demonstrate a redox-based resistive switch exploiting the formation of conductive filaments in a bulk silicon-rich silicon oxide. Resistive switching is intrinsic to silicon oxide layer and does not depend on the diffusion of metallic ions to form conductive filaments.

Devices exhibit multi-level switching and analogue modulation of resistance as well as standard two-level switching. We demonstrate both operational modes (bipolar and unipolar switching modes) that make it possible to dynamically adjust device properties, in particular two highly desirable properties: non-linearity in I-V curves and self-rectification.

Scanning tunnelling microscopy (STM), atomic force microscopy (AFM), and conductive atomic force microscopy (C-AFM) measurements provide a more detailed insight into both the location and the dimensions of the conductive filaments. In addition, we report on the material changes leading to resistive switching confirming that protrusions formed at the surface of samples during switching are bubbles, which are likely to be related to the outdiffusion of oxygen.

We discuss aspects of conduction and switching mechanisms and we propose a physical model of resistive switching. We demonstrate room temperature quantisation of conductance in silicon oxide resistive switches, implying ballistic transport of electrons through a quantum constriction, associated with an individual silicon filament in the SiOx bulk. In addition we suggest that the conductance quantum, $G_0$, is a natural boundary between the high and low resistance states of our devices.
The development of conventional non-volatile memories is coming to a halt and novel approaches are being intensively pursued. The recent realization of memristors, nanodevices exhibiting non-volatile resistive switching, could be crucial in this endeavor, when used as Resistive Random Access Memories (ReRAMs). ReRAMs can be fabricated in a simple structure allowing high-density implementation, have low-power operation as well as fast switching and large retention times. Furthermore, they are compatible with conventional CMOS technology.

In this work we present nonvolatile resistive switching in Ag2S and MgO-based structures. Ag2S thin films were fabricated using three different methods (sputtering, sulfurization, electrodeposition) aiming to optimize and select the appropriate processes. The composition of the fabricated set of samples was found to strongly depend on the used processes. The resistive switching characteristics associated with the Ag2S system was obtained and different behaviors were observed in the devices depending on the measuring and fabrication conditions.

On the other hand, MgO structures were fabricated from a monocrystalline target using magnetron sputtering. The full Pt/MgO/Ta/Ru (150/15/20/5 nm) stacks were defined using a shadow mask with circle-shaped apertures of 300 µm in diameter. These devices exhibit nonpolar resistive switching without the need of an electroforming step, contrarily to commonly reported in such devices. We have found that the high resistance state (HRS) shows a space charge limited current (SCLC) mechanism, while the low resistance state (LRS) shows ohmic behavior, which could be indicative of the formation of Mg filaments between the top and bottom electrodes. We have also shown that the LRS resistance is inversely proportional to the current compliance used during the SET process, and that a too high current compliance will switch the device permanently ON.
Transfer torque magnetic tunnel junction (STT-MTJ, the STT-MRAM cell) behavior and its possible use to implement learning-capable synapses. Three programming regimes (low, intermediate and high current) are identified and compared. System-level simulations on a task of vehicle counting highlight the potential of the technology for learning systems. Monte Carlo simulations show its robustness to device variations. The simulations also allow comparing system operation when the different programming regimes of STT-MTJs are used. In comparison to the high and low current regimes, the intermediate current regime allows minimization of energy consumption, while retaining a high robustness to device variations. These results open the way for unexplored applications of STT-MTJs in robust, low power, cognitive-type systems.

13:00 – 14:00
Lunch Break

14:00 – 14:30

Alex Serb, “The right tool for the right job: developing tools to overcome the RRAM testing bottleneck.”

RRAM technology is currently a hot research topic with potential applications ranging from industrial-grade memory to neuromorphic artificial synapse arrays. With a plethora of materials to choose for the construction of the active layer and electrodes of the device many groups in the world work towards the goal of developing the ultimate resistively switching device. However, testing of the constantly evolving devices is still largely hampered by the lack of instruments specifically designed to test them in a quick & dirty way: accurate enough to give an indication as to whether research is progressing in the correct direction and crucially: fast.

In this talk we discuss the art of testing resistively switching devices and cover the efforts carried out at the University of Southampton towards automating the procedure. We present an in-house-developed instrument designed to mitigate the sneak path problem, implement cut-off type current compliance, mass test the array (e.g. reading 1024 devices in < 1’) and run via an in-house-designed, user-friendly interface. The instrument software includes standardised testing routine modules designed to allow the unsupervised operation of the system for extended periods of time, as well as carry out unconventional experiments. Examples of results generated by the system under various testing conditions are shown.

The talk concludes with projected future developments for our instrument and an outlook on our continuing efforts to devise a generalised framework for automated testing of resistively switching devices.
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Large attention has been recently given to a novel technology named memristor, for having the potential of becoming the new electronic device standard. Memristors are dynamic nanoscale electron devices that are nowadays regarded as a promising solution for establishing next-generation memory, owing to their potential of achieving “more” (functionality/information storage) for “less” (power and physical dimensions). Most interestingly, it has been envisioned that mimicking the functionality of biological brain systems will fulfil its potential. During this talk, I will present how memristors can be exploited in practical applications, with particular emphasis in the areas of analogue IC design and neuromorphic systems.

There is nowadays a regain of interest in neuromorphic computing which is mainly due to predicted end of scaling of the complementary metal oxide semiconductor (CMOS) technology. It is known that this shortcoming can be compensated through the usage of alternative technologies and computing solutions such as brain-like computing systems. However, the main challenge of utilizing potentials of artificial neural networks for high-performance information processing, is a lack of suitable hardware. Indeed, practical neural networks rely on very large number of synapses, high connectivity between neurons, and high computational parallelism, and conventional CMOS technology is inadequate in meeting these goals. The particular challenge is that the synapse is an analog memory element and CMOS implementations are too bulky even when realized with custom circuits. Inspired by this observation, we have started looking for a solution in other newly emerged but promising device technologies such as memristive devices and floating-gate transistors that behave similarly to biological synapses.

In this direction, recently we have demonstrated experimentally that each of these devices, i.e. memristive devices and floating-gate transistors, can be used for the hardware implementation of neuromorphic systems which are originally developed for pattern classification application. First, we fabricated an analog 12x12 memristor crossbar and for the first time we showed that after training it is capable of classifying 3x3-pixel images. Next, we conducted the same experiment, but in much larger scale, using floating-gate transistors having the application of handwritten digit classification using the MNIST database in mind. In this talk we would present some of the most recent results of these two experiments.
10:30 – 11:00 Morning Break

11:00 – 11:20

Daniele Ielmini, ‘Logic computing with resistive switching devices’

Resistive switching (RS) technology is one of the most mature candidate memory technologies as high density storage class memory (SCM) and embedded memory. While the memory applications are being considered by the semiconductor industry, novel concepts for RS in computing are emerging. This talk will review RS logic in terms of logic gate operation, area scaling and power consumption. In particular, RS will be shown to enable a virtual suppression of off-state power consumption due to the normally-off operation, while a 100x reduction of circuit area is predicted thanks to the 2-terminal RS structure and the small number of switch per operation. The reliability challenges to compete with CMOS and beyond-CMOS concepts will be finally addressed.

11:20 – 11:40

Georgios Sirakouilis, ”Methodology for design of memristor-based circuits on Nano/CMOS hybrid crossbar architecture.”

The crossbar architecture is viewed as the most likely path towards novel nanotechnologies which are expected to continue the technological revolution. Memristor-based crossbars for integrating memory units have received considerable attention, though little work has been done concerning the implementation of logic. In this talk we focus on memristor-based complex combinational circuits. Particularly, we present a design methodology for digital circuits. The proposed methodology follows a CMOS-like design scheme which can be used for the efficient design and mapping of digital circuits onto the memristor-based crossbar geometry. For their implementation, a hybrid nano/CMOS crossbar type with memristive cross-point structures and available transistors is elaborated, which is a promising solution to the interference between neighboring cross-point devices during access operation. Circuit functionality of the presented circuits is exhibited with simulations conducted using a simulator environment which incorporates a versatile memristor device model. The proposed design and implementation paradigm constitutes a step towards novel computational architectures exploiting memristor-based logic circuits, and facilitating the design and integration of memristor-based circuits with nanoelectronics applications of the near future.
Neuromorphic designs are a promising area of application for memristors. The key advantages of memristors from point of view of neuromorphic designs are their nonvolatility and scalability filling the requirement for analog design friendly memory. On the other hand uncertainty remains about repeatability and endurance of memristors.

In our talk we consider one possible area of application of memristors for emulation of plasticity in neuromorphic neural networks. The talk will outline our research vision and present first simulation results with modelling plastic designs with ECM memristors.

Resistive switching phenomena in metal-oxide-based material systems have been largely studied for future generation of non-volatile RRAM memories, and recently are receiving an increasing interest towards new type of applications, such as reconfigurable logic and synaptic electronics. This talk will review recent our advancements on memristive devices based on HfO2 and doped-HfO2. The oxide layers (binary and doped oxides, ≈5 nm thick) are deposited by atomic layer deposition and the resistive switching properties are analysed from micro- to nanoscale in metal/oxide/metal devices as well as through conductive atomic force microscopy to address the device performance versus materials properties. Furthermore, in view of application of these devices as synaptic elements, the long term plasticity, as potentiation and depression typical of biological synapses, are characterized by various pulsed operation schemes. Special emphasis is given to programming algorithms based on a train of identical pulses, and to achieve an analogue modulation of the device conductance.

Perspectives for 3D integrated heterogeneous systems including memristor-based blocks
14:00 – 15:00  Individual WG Meeting Discussions
15:00 – 15:30  Round Table Discussion on “Memristor Proposals within H2020 and Elsewhere”
15:30 – 16:00  Coffee Break
16:00 – 18:00  One-on-one Meetings for Collaborations/Research Coordination